

CLAIMS

1. A thin film capacitor for reducing power source noise connected to a power source for reducing power source noise, characterized in that

said capacitor has a dielectric thin film,

said dielectric thin film is comprised of a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, and

said bismuth layer structured compound is expressed by the formula $(\text{Bi}_2\text{O}_2)^{2+}(\text{A}_{m-1}\text{B}_m\text{O}_{3m+1})^{2-}$ or $\text{Bi}_2\text{A}_{m-1}\text{B}_m\text{O}_{3m+3}$, where the symbol m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W.

2. The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor is a decoupling capacitor connected in parallel between the power source and an integrated circuit.

3. The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor is a bypass capacitor connected in parallel between the power source and an integrated circuit.

4. The thin film capacitor for reducing power source noise as set forth in claim 2 or 3, wherein said capacitor is arranged near an integrated circuit chip.

5. The thin film capacitor for reducing power source noise as set forth in any one of claims 2 to 4, wherein said capacitor is arranged in contact with an integrated circuit chip.

6. The thin film capacitor for reducing power source noise as set forth in any one of claims 2 to 4, wherein said capacitor is arranged between an integrated circuit chip and a circuit board.

7. The thin film capacitor for reducing power source noise as set forth in any one of claims 2 to 4, wherein said capacitor is mounted buried in a recess of a circuit board.

8. The thin film capacitor for reducing power source noise as set forth in any one of claims 2 to 4, wherein said capacitor is mounted on the surface of a circuit board.

9. The thin film capacitor for reducing power source noise as set forth in any one of claims 2 to 4, wherein said capacitor is formed integrally inside a circuit board.

10. The thin film capacitor for reducing power source noise as set forth in any one of claims 2 to 4, wherein said capacitor is arranged at an inside or surface of a connection socket.

11. The thin film capacitor for reducing power source noise as set forth in any one of claims 1 to 10, wherein said capacitor has a lower electrode formed on said thin film forming substrate, said dielectric thin film formed on said lower electrode, and an upper electrode formed on said dielectric thin film.

12. The thin film capacitor for reducing power source noise as set forth in any one of claims 1 to 10, wherein said capacitor has a multilayer structure comprised of a plurality of said dielectric films stacked via electrodes.

13. The thin film capacitor for reducing power source noise as set forth in any one of claims 1 to 10, wherein said capacitor is comprised of a bismuth layer structured compound having a c axis orientation of at least 80%.